Quantum Computing with Very Noisy Gates

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- The C_4/C_6 architecture.
- Performance data from simulation.
- Resource requirements.

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Fault-Tolerant Quantum Computing

- **Requirement 3 for scalable QC[a] implementation:**
  Sufficiently low noise affecting physical gates and memory.

DiVincenzo (2000) [4]

- *Error model*: The type of noise affecting a QC implementation.
- *Fault-tolerant architecture*: A scheme for scalable QC in the presence of noise.

- Fundamental problems of FTQC[b]:
  1. Scalable QC with error model $\mathcal{E}$?
  2. Scalable QC with fault-tolerant architecture $\mathcal{A}$ and with $\mathcal{E}$?

- Practical problems of FTQC[b]:
  1. Can computation $\mathcal{C}$ be implemented with a given error and device budget?

[a] Quantum Computing. [b] Fault-Tolerant Quantum Computing

On Noise Thresholds

Fault-Tolerance Threshold Theorem.

- Thresholds depend on:
  - Error model
  - Available devices.
  - Geometrical constraints.
  - ...

$$\vec{0} \leq \text{threshold} < \vec{1}$$

- Threshold studies yield:
  - Fault-tolerant engineering strategies.
  - Guidelines for gate-error/geometry/resource trade-offs.

- Thresholds are asymptotic.
  - Thresholds are not “observable”.

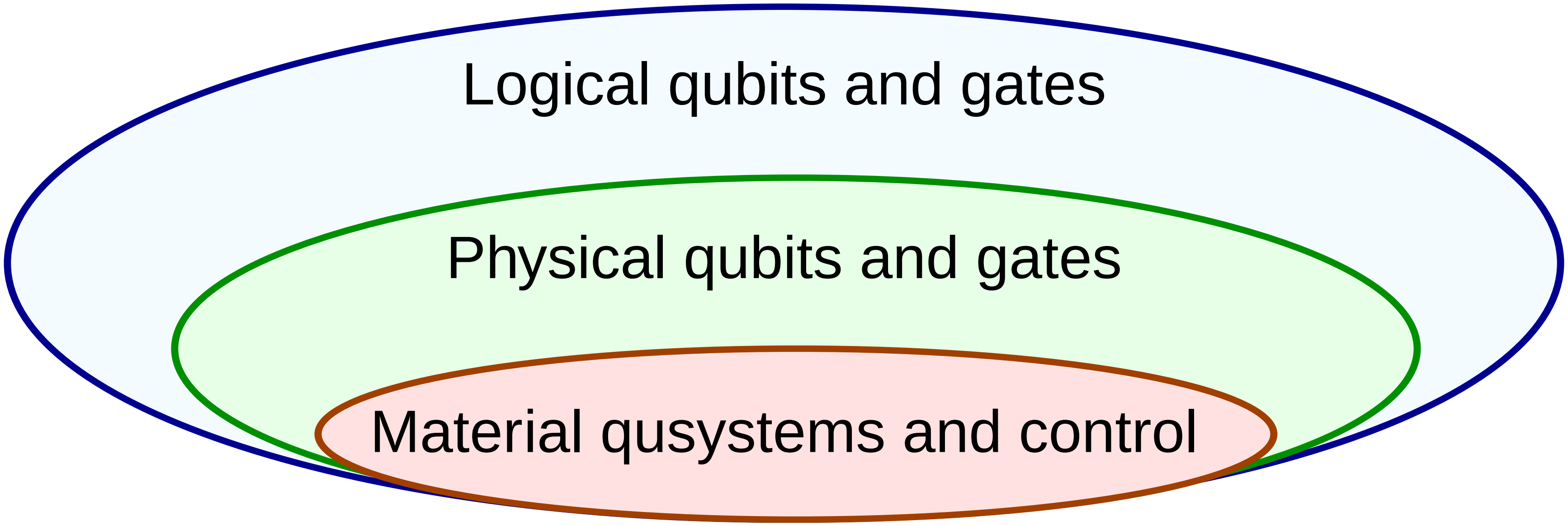
- Thresholds hide resource tradeoffs.

In Other Words...

- Thresholds are too optimistic.
  - Error budget near threshold $\rightarrow$ impractical resources.
  - ... try to do better by one to two orders of magnitude.

- Thresholds are too pessimistic.
  - Most bounds/estimates are based on specific, concatenated architectures.
  - Large computations/simulations/fundamental tests may be implementable anyway.
    E.g. rare-error kickback may be deferred.
  - ... there is no non-idealized threshold.

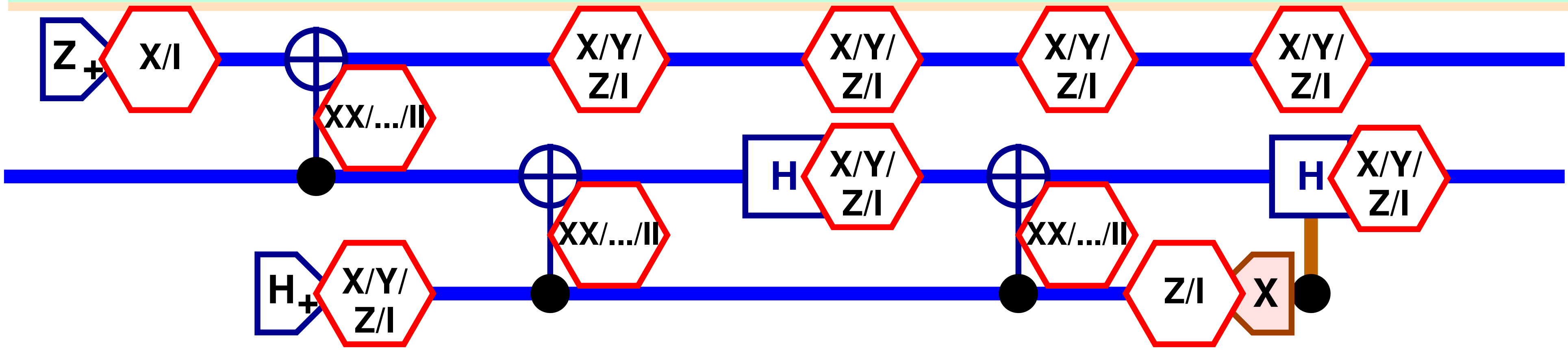
Constructing Quantum Computers



- Fault-tolerant architectures:
  physical qubits,gates $\Rightarrow$ near-perfect logical qubits, gates.

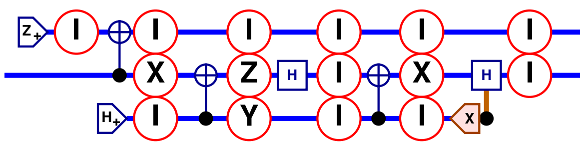
- Common structural assumptions:
  - Remaining errors are not removable by physical engineering.
  - Physical qubits and gates are nearly independent.
  - Physical gates can be applied in parallel.
  - Any number of physical qubits can be used, subject to geometrical constraints.

Error Models I



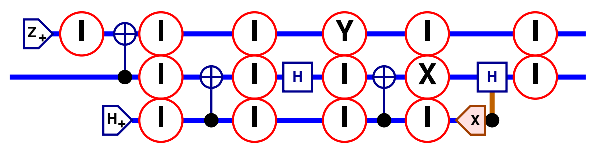
- General error expansion:

$$\sum \ldots +$$



$$\otimes \left| e_a \right\rangle$$

$$\ldots + \ldots$$



$$\otimes \left| e_c \right\rangle + \ldots$$

$$= \sum_e \sum_{\mathbf{p}=(p_i)_i} \underbrace{\left| e_{\mathbf{p}} \right\rangle_{\text{Env}}}_{\text{Unnormalized ``environment'' state}} \prod_i \overbrace{G_i}^{\text{Gate } i} \underbrace{E_i(p_i)}_{\text{Pauli product at location } i}$$

Error Models II

$$= \sum_e \sum_{\mathbf{p}=(p_i)_i} \underbrace{|e_{\mathbf{p}}\rangle_{\text{Env}}}_{\text{Unnormalized ``environment'' state}} \prod_i \overbrace{G_i}^{\text{Gate } i} \underbrace{E_i(p_i)}_{\text{Pauli product at location } i}$$

- Assume temporal and spatial independence:

  Total amplitude of errors simultaneously affecting k given locations decays exponentially with k.

- Further idealizing assumptions:
  1. Errors are probabilistic Pauli ($|e_p\rangle$ are orthogonal).
     Justification: The randomization conjecture.
  2. Errors at different locations are statistically independent.
     Justification: Increase physical separations or delocalize logical qubit encodings.

Two Error Trade-offs

- Preparation and measurement error requirements are benign.

  Justification: Given good CNOTs, use classical error-correction and detection methods to reduce preparation and measurement errors.

- Long "measurement" times and feed-forward delays require very good quantum memories.

  Explanation: Feedforward circuits require delaying for measurement outcomes.
  Note: Feedforward loop does not require amplifying the measurement outcome for human consumption.

  $$\text{(memory error rate)} * \text{(feed-forward delay)} \ll 1.$$

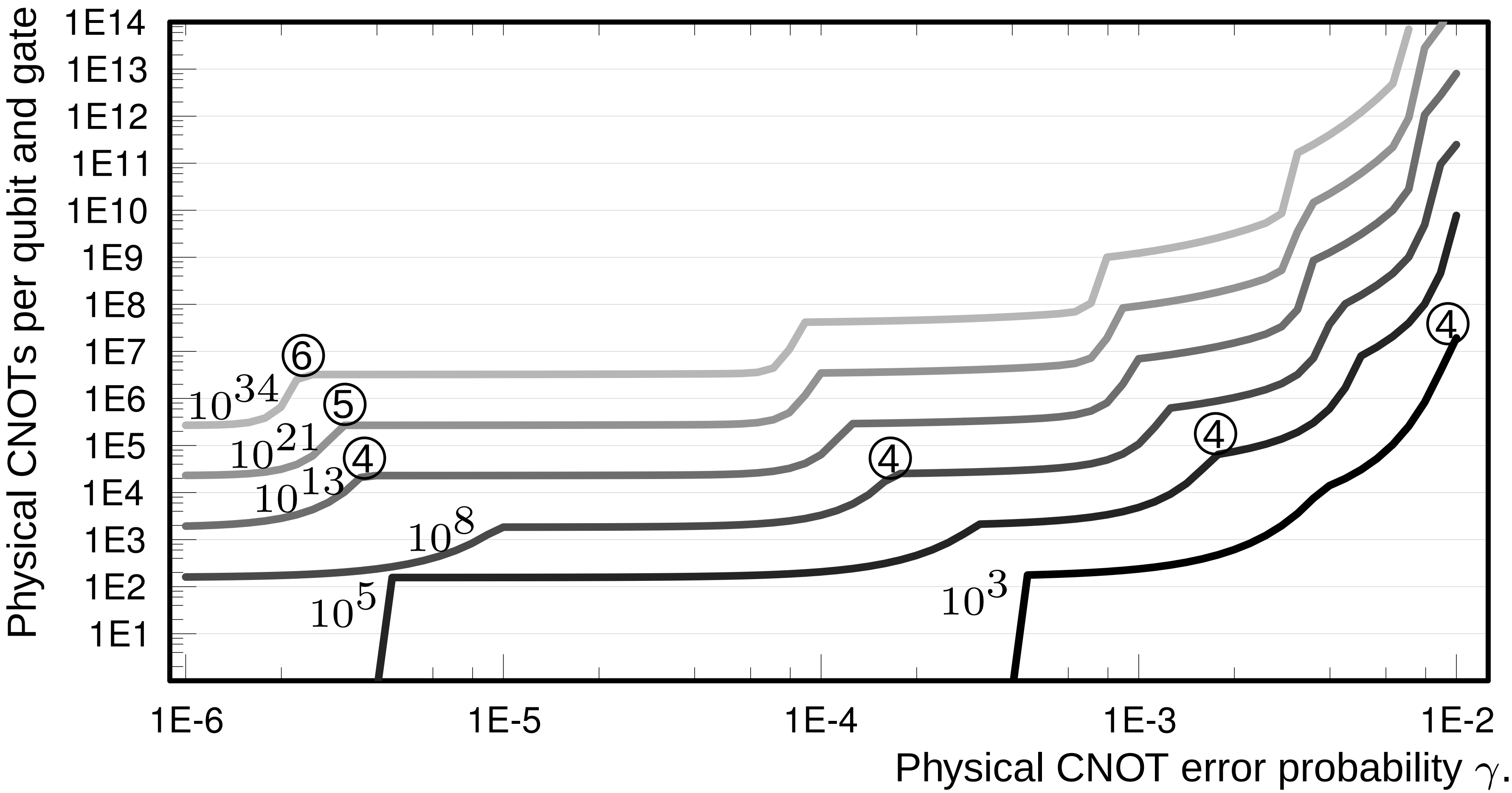
The C_4/C_6 Architecture: Features

- Use the simplest error-detecting codes and concatenation.
- Exploit error-correcting teleportation.
- Postselected quantum computing for state preparation.
- Partial decoding for state preparation.
- Fault-tolerant implementation of Clifford gates $+\ \delta$ suffices.

- Evidence that depolarizing errors $> 3\%$ per CNOT* are ok.

* error ϵ/CNOT $\equiv \frac{4\epsilon}{5}$/one-qubit gate, $\frac{4\epsilon}{15}$/preparation or measurement, no geometrical constraints.

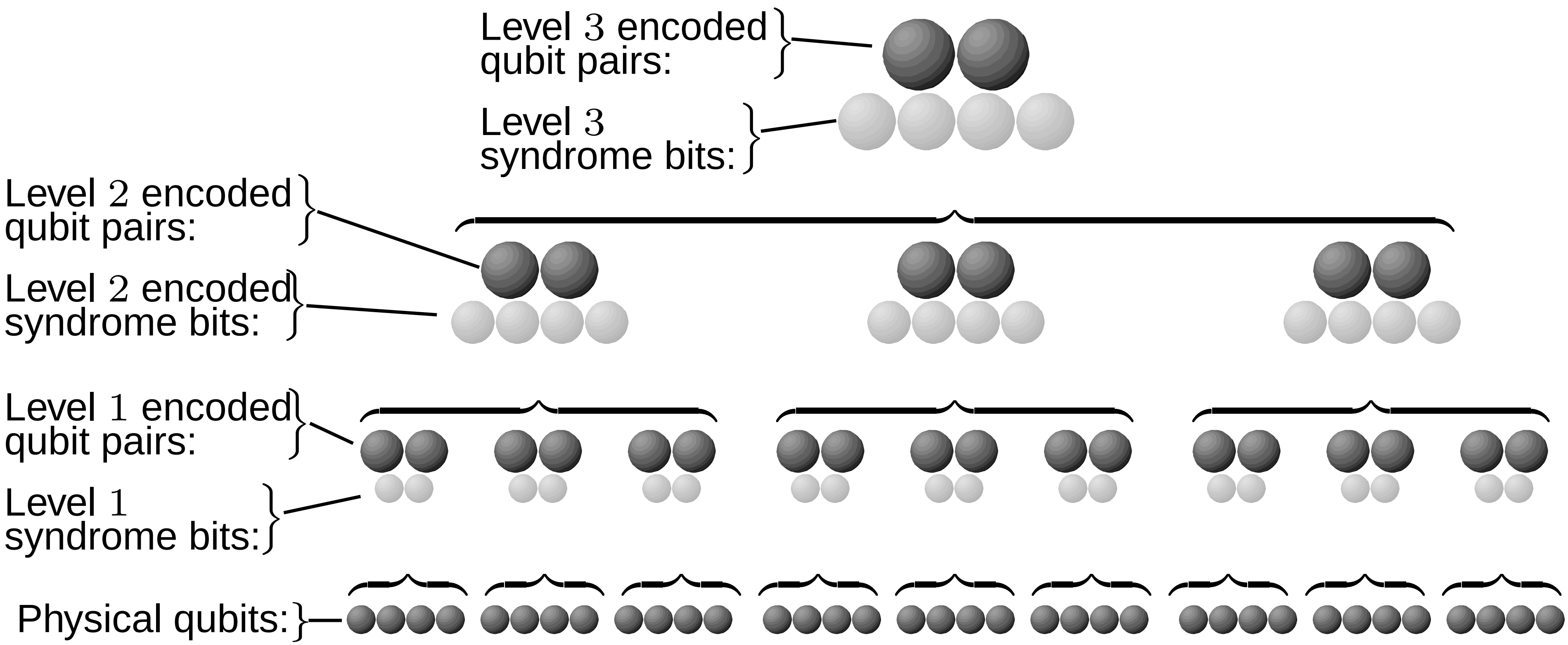
Typical Resource Requirements



- Resource overheads* for the C_4/C_6-architecture and different computation sizes (by simulation and modelling).

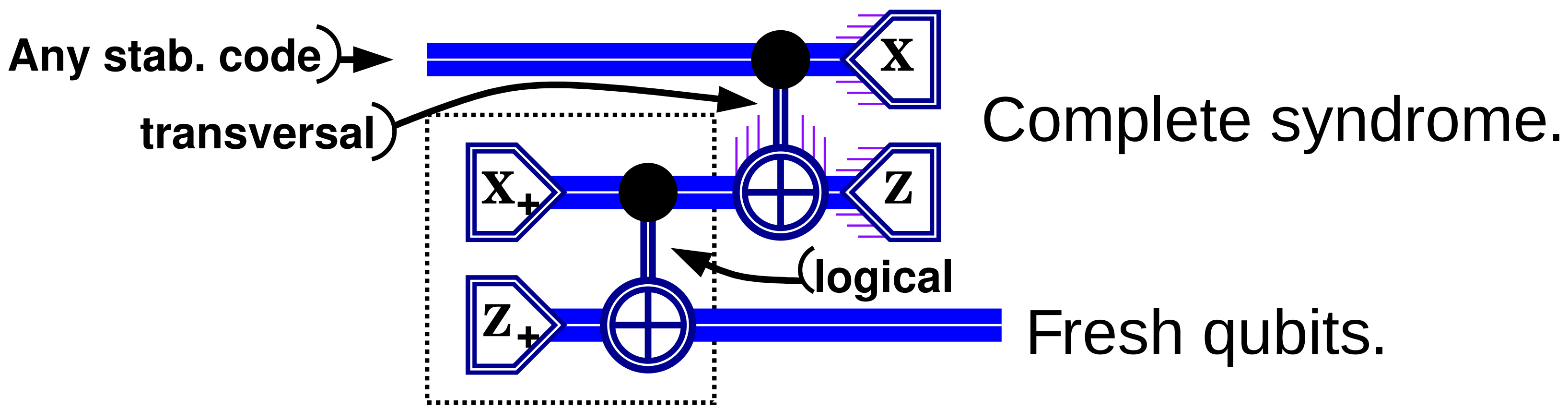
* Order-of-magnitude, extrapolated.

C_4/C_6 concatenation hierarchy.



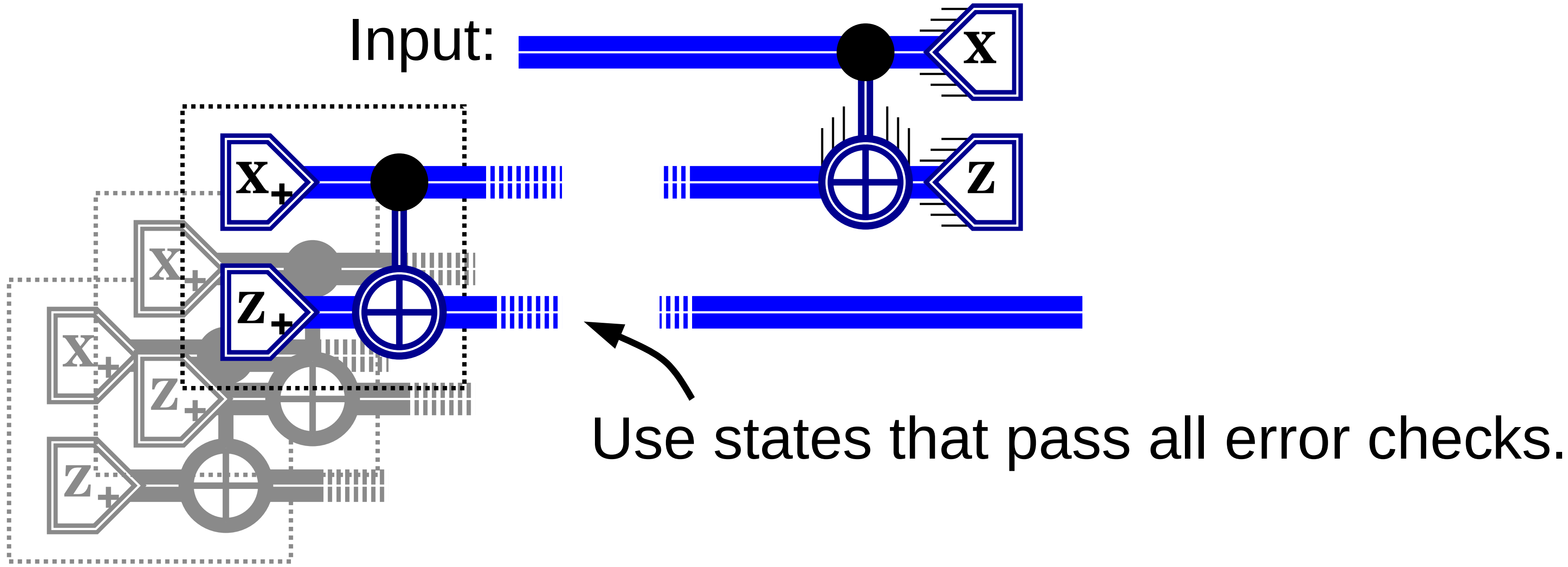
Error-correcting Teleportation

- Syndrome measurement from qubit-wise teleportation.



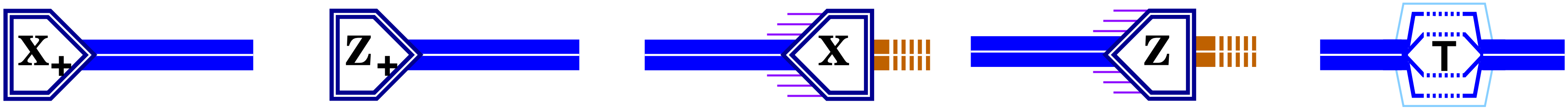
- Syndrome $\longrightarrow$ error detection, correction, tracking.
- Use *Pauli frame* to avoid explicit correction gates.

Post-selected State Preparation

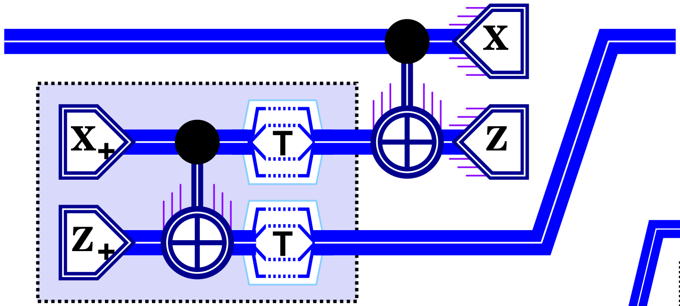


- Error in the prepared state $\equiv$ error in the input state.
- States only need to be "good" conditional on error checks.
  - Residual errors $+$ input $+$ Bell measurement errors must be correctable.
- Can use parallel state preparation factories.

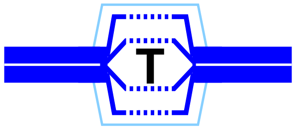
C_4 Bell-State Preparation



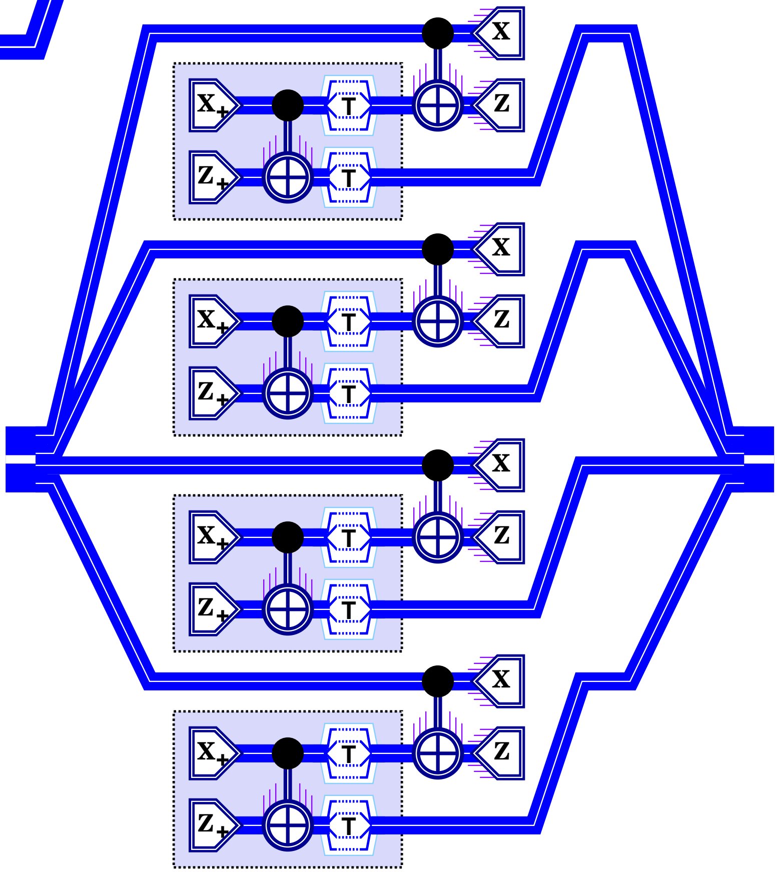
Logical qubits teleportation:



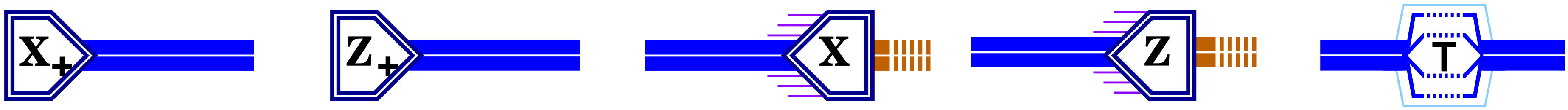
Implementations:



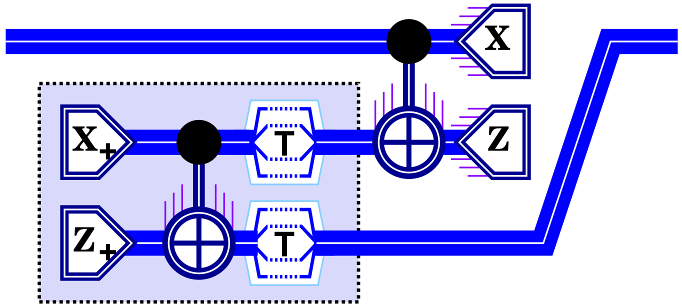
$\Rightarrow$



C_4 Bell-State Preparation



Logical qubits teleportation:



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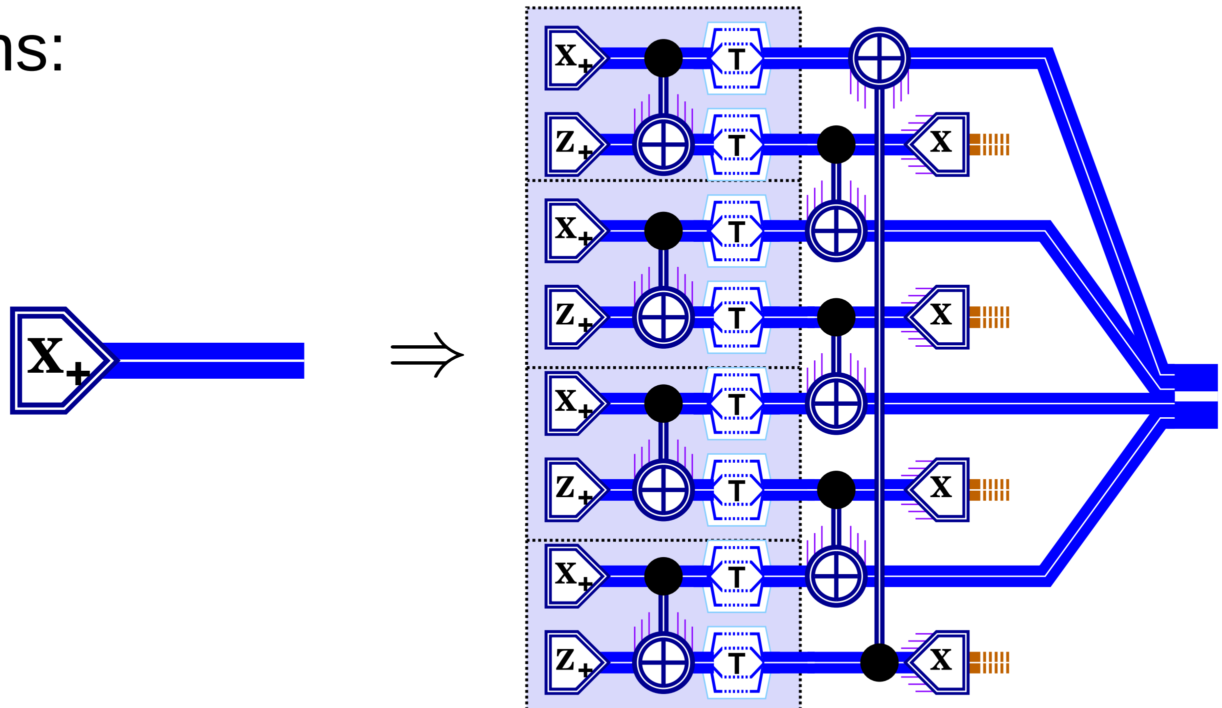
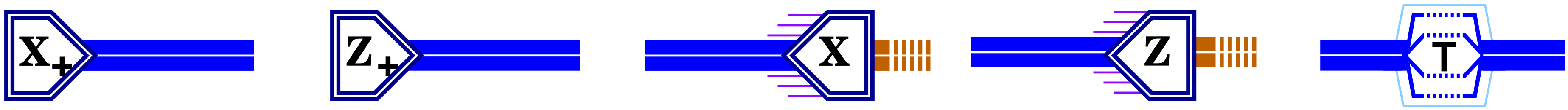
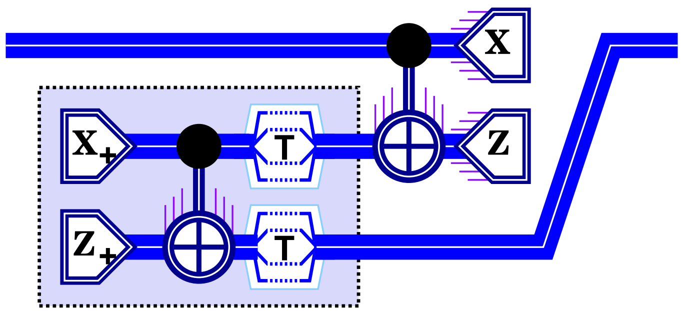


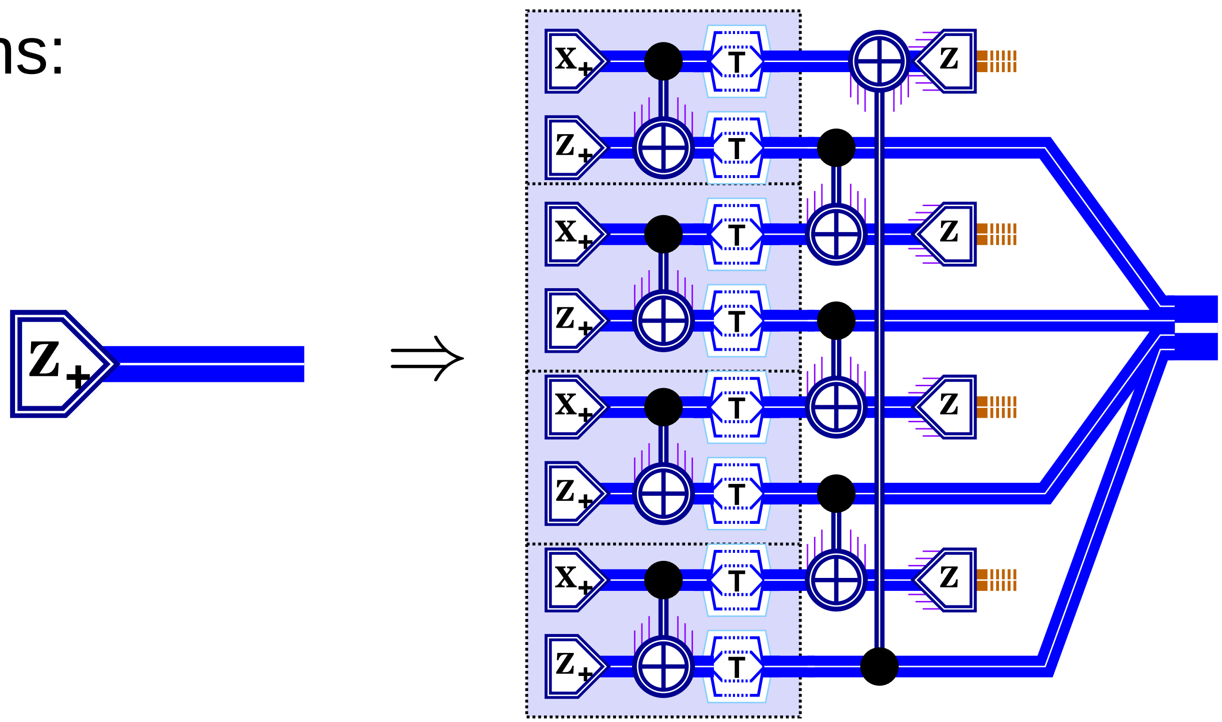
C_4 Bell-State Preparation



Logical qubits teleportation:



Implementations:



Postselected Quantum Computing

- Postselected quantum computers.
  - Can execute any of the basic operations, but
  - an operation may fail, possibly destructively.
  - If an operation fails, this is announced.

  ...exponentially small success probability (not 0) is possible.

- A postselected QC is fault-tolerant if

  success $\longrightarrow$ negligible probability of error.

- A postselected FTQC only needs to detect errors.

- Does postselected FTQC imply FTQC?

  ...Nearly: Use postselected FTQC to prepare key states.

Power of Clifford-Pauli Operations

- The CSS operations, $\mathcal{CSS}$:
  Preparation of $|0\rangle$ and $|+\rangle$, CNOT, measurement of X and Z.
  - CSS operations suffice for encoding/decoding CSS codes.

- Universal quantum computation is possible with $\mathcal{CSS}$, H and $|\pi/8\rangle$-preparation.

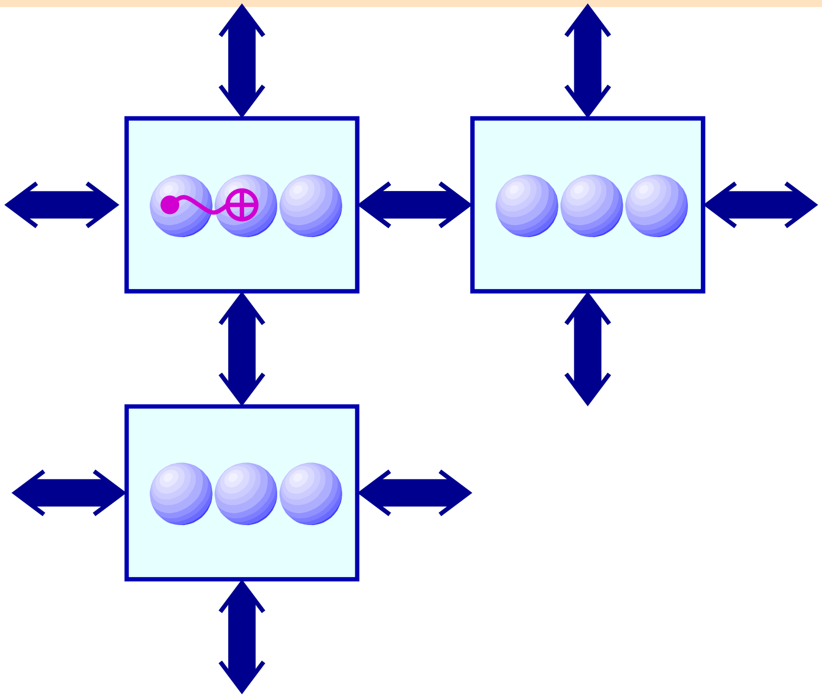
$$\text{QC} = \overbrace{\mathcal{CSS} + \underbrace{\text{``}\epsilon\text{''}}_{H}}^{\subseteq\mathcal{N}} + \underbrace{\text{``}\delta\text{''}}_{|\pi/8\rangle}.$$

- A fault-tolerant computation strategy:
  1. Implement a fault tolerant CSS computer, i.e. arbitrarily accurate logical $\mathcal{CSS}$ with feedforward.
  2. $+\text{``}\epsilon\text{''} + \text{``}\delta\text{''}\ldots$

$+\text{``}\delta\text{''}$: $|\pi/8\rangle$ purification using good $\mathcal{CSS} + \text{''}\epsilon\text{''}$
Bravyi&Kitaev (2004) [1], Knill (2004) [2]

- FT$\mathcal{CSS}$ and ($|\pi/8\rangle$ error) $\leq$ ($|0\rangle$, $|+\rangle$ error) $\Rightarrow$ FTQC?

In Other Words...



1. Build a device that supports a very good CSS-based (or similar) quantum memory for (say) three logical qubits.

2. Ensure that neighboring devices can exchange logical qubits.

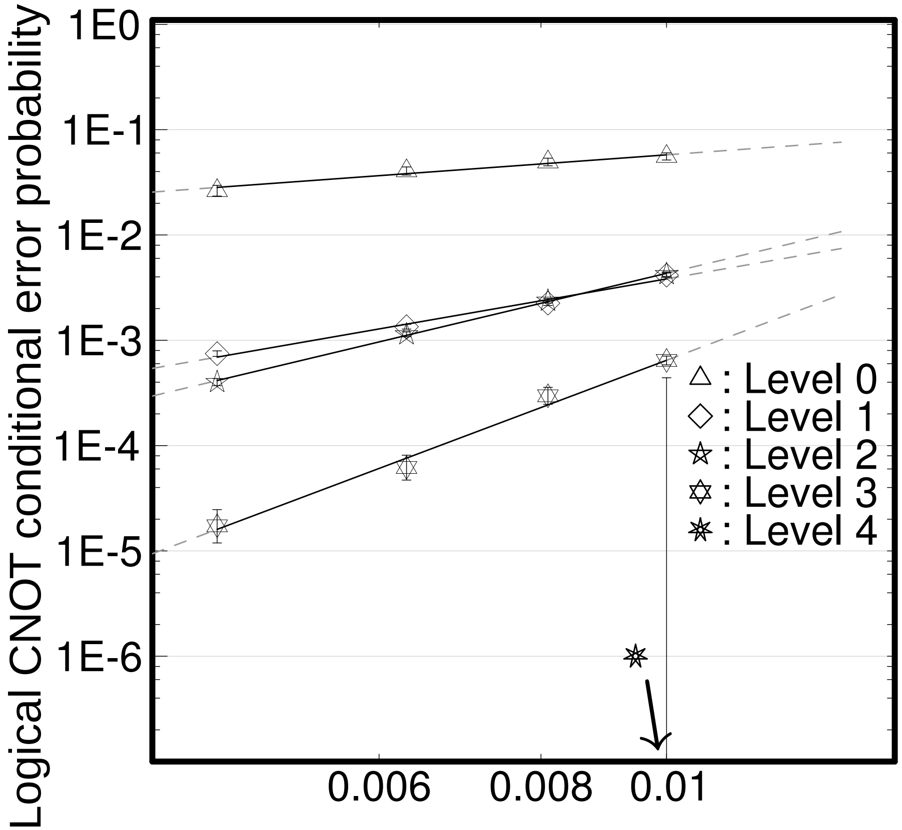
3. Implement quantum gates internally to a device at leisure.
   $\Rightarrow$ the devices can form a quantum computer.

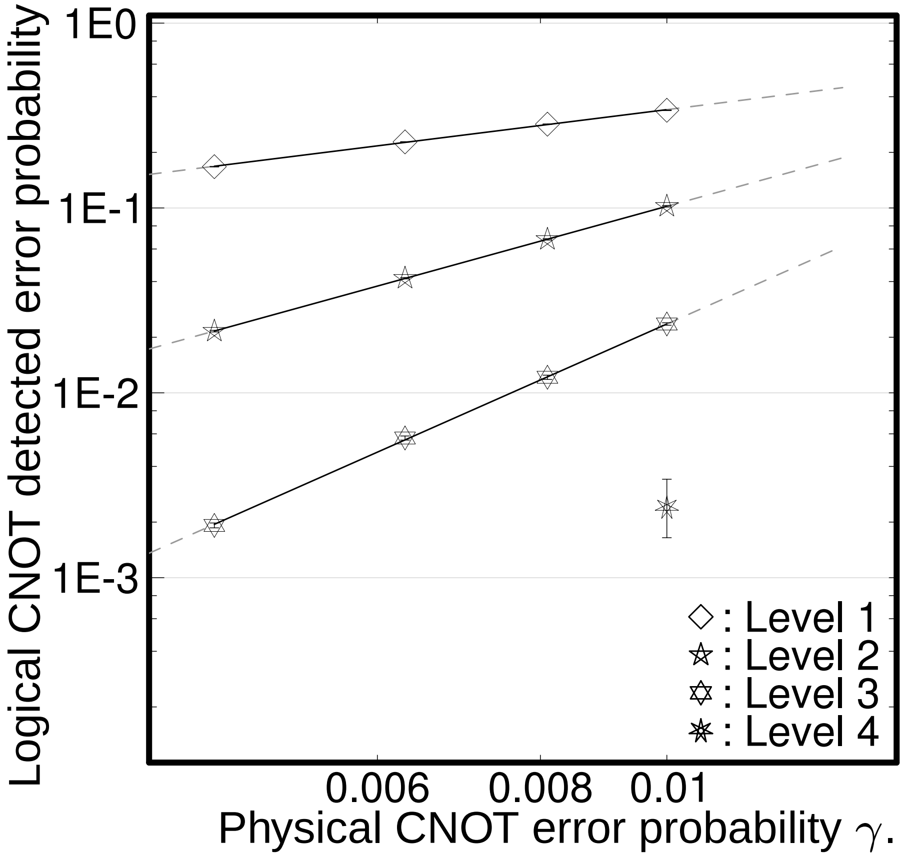
Simulation of the C_4/C_6 Architecture

1. Computer-assisted heuristics to arbitrarily high levels.
   - Error-model propagation to detect rare-error kickbacks.
2. Monte-Carlo simulation to determine C_4/C_6 error behavior up to level 4.

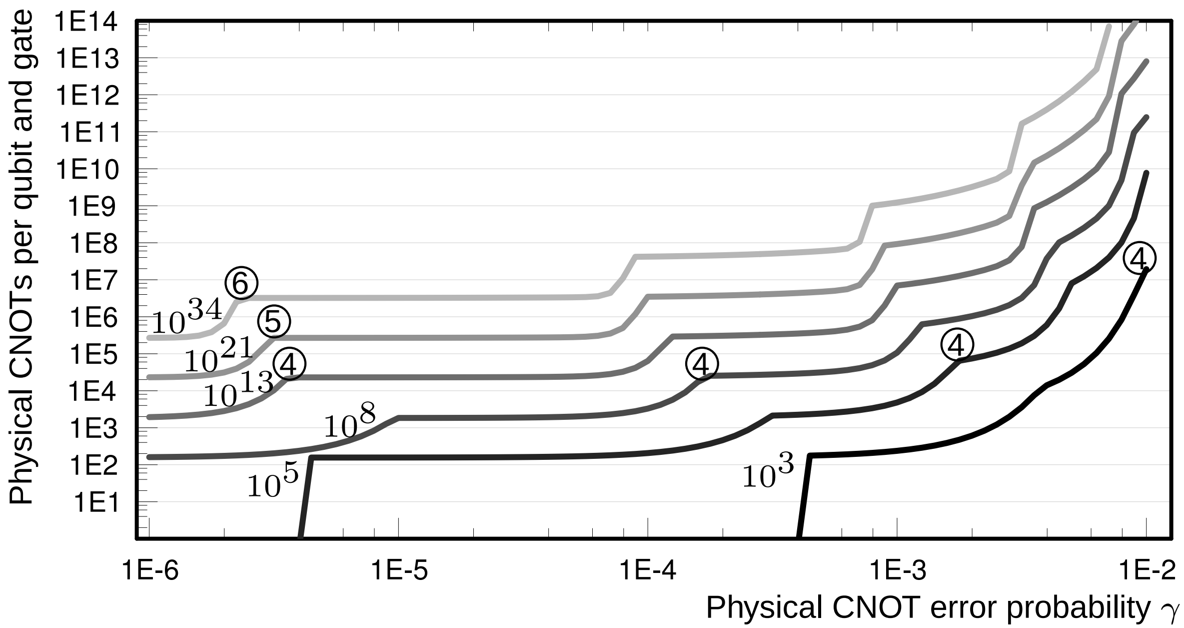
   Implementation issues:
   - Avoid transients:
     Verify error behavior of the second operation.
   - Verify full error behavior:
     Operate on one-half of an entangled pair.
   - Verify that errors do not compound:
     Check on a long sequence of operations.
   - Architecture is not strictly concatenated:
     Full simulations at high levels.
   - Keep track of resources used.

Error Probabilities for Scalable QC





Conclusion



- Can my computation (or simulation or fundamental test) be implemented with a given error and device budget?

Contents

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